QUALITY SEMICONDUCTOR, INC.

Guaranteed Low Skew CMOS Clock Driver/Buffer

QS5807T
QS52807T

FEATURES/BENEFITS

- 10 output, low skew clock signal buffer
- TTL output voltage swing
- 25Ω on-chip resistors available for low noise
- Input hysteresis for better noise margin
- Guaranteed low skew
  - 0.35ns same transition
  - 0.45ns opposite transition
  - 0.75ns different devices
- Industrial temperature range
- Available in QSOP (Q) and SOIC (SO)

DESCRIPTION

The QS5807T clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS5807T generates ten non-inverting outputs. Designed in QSI's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.35ns for same-transition, same-bank signals. The QS52807T has on-chip series termination resistors for lower noise clock signals. The series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. See Application Note AN-21 for more information on low-skew clock buffers.

Figure 1. Functional Block Diagram

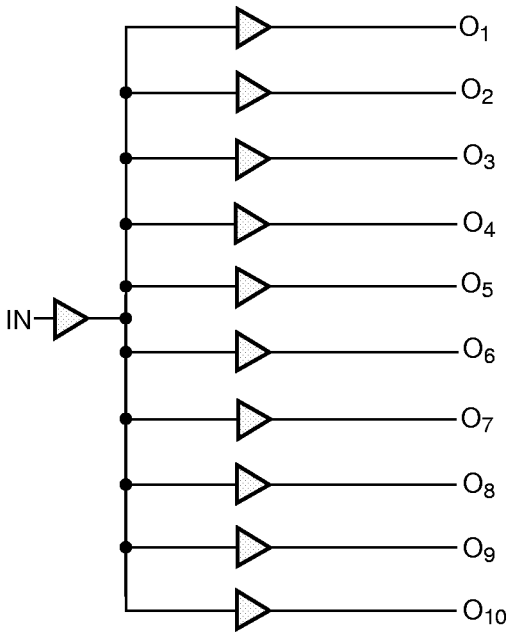


Figure 2. Pin Configurations

(All Pins Top View)

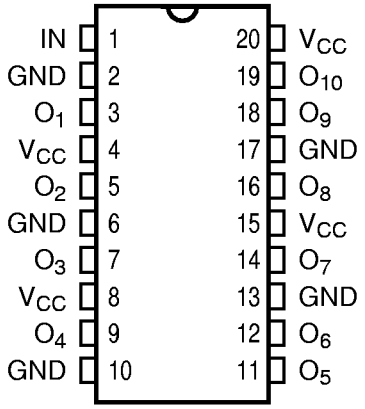


Table 1. Pin Description

Name	I/O	Description
IN	I	Clock Input
$\overline{IN}$	O	Clock Outputs

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation At T_A = 85°C, QSOP	0.82 watts
SOIC	0.75 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

	QSOP		SOIC		
Pins	Typ	Max	Typ	Max	Unit
C_{IN}	3	6	5	7	pF

Note: Capacitance is characterized but not tested.

Table 4. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for All Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage QS5807T	V_{CC} = Min., V_{IN}=V_{IH} or V_{IL}, I_{OH} = –15mA	2.4	3.3	—	
		I_{OH} = –32mA	2.0	3.0	—	
V_{OH}	Output HIGH Voltage QS52807T	V_{CC} = Min., V_{IN}=V_{IH} or V_{IL}, I_{OH} = –8mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage QS5807T	V_{CC} = Min., V_{IN}=V_{IH} or V_{IL}, I_{OL} = 48mA	—	0.2	0.50	V
V_{OL}	Output LOW Voltage QS52807T	V_{CC} = Min., V_{IN}=V_{IH} or V_{IL}, I_{OL} = 8mA	—	—	0.50	V
$\lvert I_{IN} \rvert$	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	—	—	1	µA
I_{OS}	Short Circuit Current(2,3)	V_{CC} = Max., V_{OUT} = GND	–60	—	–250	mA
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
R_{OUT}	Output Resistance(4) QS52807T	V_{CC} = Min., I_{OL} = 12mA	—	28	—	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
3. Guaranteed by design but not tested.
4. Output resistance represents the total output impedance of the logic device and includes added series termination resistance.

Table 5. Power Supply Characteristics

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions		Typ	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		0.2	1.5	mA
ΔI_{CC}	Power Supply Current Per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V Input toggling @ 50% duty cycle		0.5	2.5	mA
I_{CCD}	Dynamic Power Supply[1] Current per Output	V_{CC} = Max., outputs enabled,		0.09	0.2	mA/ MHz
I_C	Total Power Supply[2] Current Examples	V_{CC} = Max., Input @ 50% duty cycle, f_I = 10MHz	V_{IN} = V_{CC} or V_{IN} = GND	8.5	21.5	mA
			V_{IN} = 3.4V V_{IN} = GND	9.5	23	
		V_{CC} = Max., Input @ 50% duty cycle, f_I = 2.5MHz	V_{IN} = V_{CC} or V_{IN} = GND	2.5	7.0	
			V_{IN} = 3.4V or V_{IN} = GND	3.0	8.0	

Notes:

1. Guaranteed but not tested. C_L = 0pF.
2. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
   where:
   D_H = Input duty cycle
   N_T = Number of TTL HIGH inputs at D_H (one)
   f_O = Output frequency
   N_O = Number of outputs at f_O (ten)

Table 6. Switching Characteristics Over Operating Range

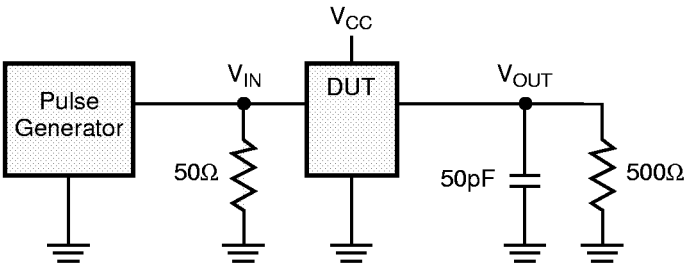
Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%
For QS5807T, C_{LOAD} = 50pF, R_{LOAD} = 500Ω. For QS52807T, C_{LOAD} = 50pF (no resistor)

			—		A		B		C		
Symbol	Description[1]		Min	Max	Min	Max	Min	Max	Min	Max	Unit
$t_{SK(O1)}$	Skew between outputs of same transition		—	0.6	—	0.5	—	0.5	—	0.35	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}-t_{PLH})	5807T	—	0.70	—	0.70	—	0.60	—	0.45	
		52807T	—	0.75	—	0.75	—	0.65	—	0.50	
$t_{SK(t)}$	Part-to-part skew[2]		—	1.0	—	1.0	—	1.0	—	0.75	
t_{PLH}	Propagation Delay[3]	5807T	1.5	4.5	1.5	4.0	1.5	3.8	1.5	3.5	
t_{PHL}	IN to Ox	52807T	1.5	5.0	1.5	4.5	1.5	4.3	1.5	4.0	
t_R, t_F	Output Rise and Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	

Notes:

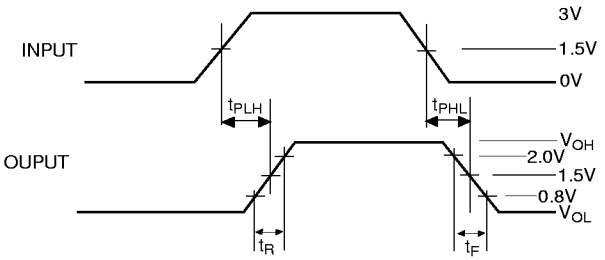
1. Skew parameters are guaranteed across temperature range, but not production tested. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. $t_{SK(t)}$ only applies to devices of the same transition, same part type, same temperature, power supply voltage, loading, package and speed grade.
3. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.

Figure 3. Test Circuits and Waveforms

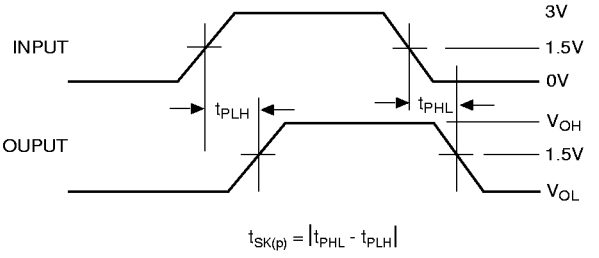


Pulse generator for all pulses: $f \leq 1.0MHz$; $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

Test Circuit

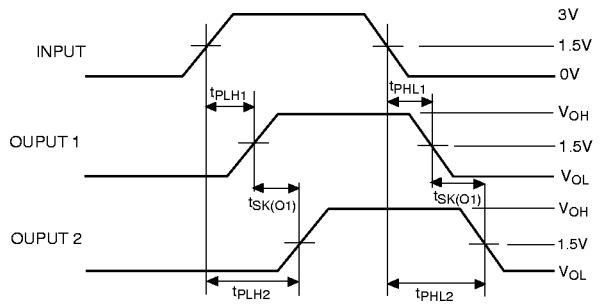


Propagation Delay



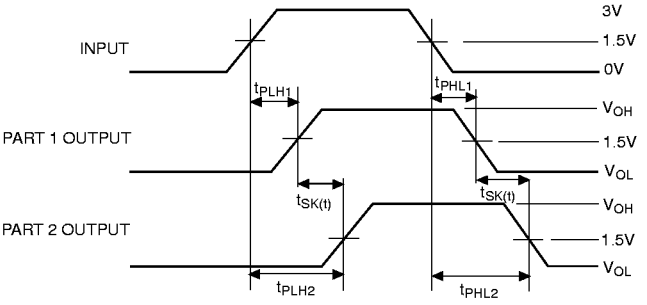
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Pulse Skew - $t_{SK(p)}$



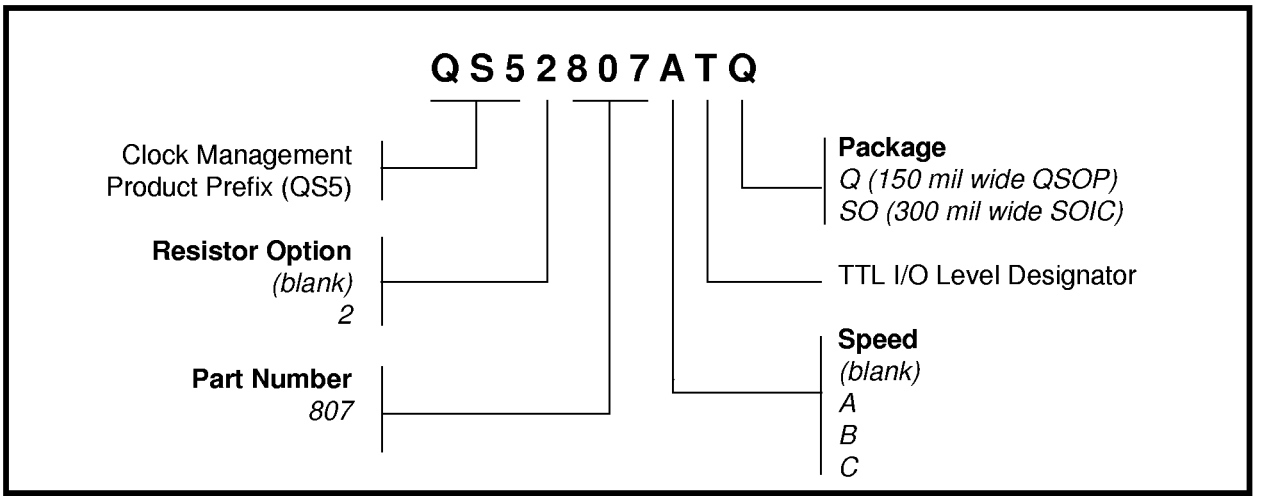
$t_{SK(O1)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew - $t_{SK(O1)}$



$t_{SK(T)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Part-to-Part Skew - $t_{SK(t)}$

ORDERING INFORMATION

Example: